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| EWULogo.png | | **EAST WEST UNIVERSITY** | |
| **Department of Computer Science and Engineering** | |
| **B.Sc. in Computer Science and Engineering Program** | |
| **Assessment 1, Spring 2021** | |
| **Course:** | | **CSE360 – Computer Architecture, Section-3** |  |
| **Instructor:** | | **Md. Nawab Yousuf Ali, PhD, Professor, CSE Department** |  |
| **Full Mark:** | | **20** |  |
| **Time:** | | **3 Hour** |  |
| **Note:** There are FIVE questions, answer ALL of them. Course outcomes (CO), cognitive levels and marks of each question are mentioned at the right margin.  XYZ is the last three digits of your ID. If your ID is 2019-3-60-125 then the value of X is1, Y is 2 and Z is 5, respectively. | | | |
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| 1. | The hypothetical machine has two instructions:  0011 = Load AC from I/O  0111 = Store AC to I/O  In these cases, the 12-bit address identifies a particular I/O device. Show the program execution (using the format of Figure 1) for the following program:   1. Load AC from device X 2. Add contents of memory location 940 3. Store AC to device Y   Assume that the next value retrieved from device 7 is Y and that location 940 contains a value of Z    **Figure 1. Example of program execution** | | [CO1, C2, Mark: 7] |
| 2. | Consider a 32-bit microprocessor, with a 32-bit external data bus, driven by a 16-MHz input clock. Assume that this microprocessor has a bus cycle whose minimum duration equals six input clock cycles. What is the maximum data transfer rate across the bus that this microprocessor can sustain, in bytes/s?  To increase its performance, would it be better to make its external data bus 64 bits or to double the external clock frequency supplied to the microprocessor? | | [CO1, C3 Mark: 2+3] |
| 3. | A microprocessor has an increment memory direct instruction, which adds 3 to the value in a memory location. The instruction has five stages: fetch opcode (four bus clock cycles), fetch operand address (three cycles), fetch operand (two cycles), add 3 to operand (five cycles), and store operand (seven cycles).  a. By what amount (in percent) will the duration of the instruction increase if we have to insert three bus wait states in each memory read and five bus wait state in memory write operation?  b. Repeat assuming that the increment operation takes 11 cycles instead of 5 cycles. | | [CO2, C3 Mark: 3+2] |
| 4. | Consider an 8-bit microprocessor to process operands and instructions. Assume that, on average, 40% of the operands and instructions are 64 bits long, 20% are 32 bits long, 20% are 16-bit long and 20% are only 8-bits long. Calculate the improvement achieved when fetching instructions and operands with the 64-bit microprocessor. | | [CO1, C3 Mark: 3] |